What is Claimed is:

1. A method of forming a copper wiring in a semiconductor device, the method comprising:

forming damascene patterns in an interlayer insulating film which is formed on a substrate;

sequentially forming a copper barrier metal layer and a copper seed layer on the surface of the interlayer insulating film including the damascene patterns;

performing a copper electroplating process to be filled the damascene patterns with a copper layer;

polishing the copper layer by means of a copper electro-polishing process to forma polished copper layer having a flat surface and a thin thickness; and

polishing the polished copper layer, the copper seed layer and the copper barrier metal layer by means of a chemical mechanical polishing process so that the surface of the interlayer insulating film is exposed, thereby forming copper wirings within the damascene patterns.

2. The method as claimed in claim 1, wherein the copper barrier metal layer is formed using one of ionized PVD TiN, CVD TiN, MOCVD TiN, ionized PVD Ta, ionized PVD TaN, CVD Ta, CVD TaN and CVD WN.

3. The method as claimed in claim 1, wherein the copper seed layer is formed using an ionized PVD method.

4. The method as claimed in claim 1, wherein the copper electroplating process comprises:

loading a wafer in which the copper seed layer is formed onto an electroplating apparatus in which a copper plating solution including an organic accelerator and an organic suppressor are added; and

setting a plating target range so that the damascene patterns could be sufficiently filled; and

applying a negative (-) power supply having current in the range of 1 ~ 5A to the wafer.

5. The method as claimed in claim 1, wherein the copper electroplating process:

loading a wafer in which the copper seed layer is formed onto an electroplating apparatus in which a copper plating solution including an organic accelerator, an organic suppressor and an organic leveler are added; and

setting a plating target range so that the damascene patterns could be sufficiently filled; and

applying a negative (-) power supply having current in the range of 1 ~ 5A to the wafer.

6. The method as claimed in claim 1, wherein the copper electro-polishing process comprises:

setting a target range similar to a target plating range for forming the copper layer, in a state that a wafer in which the copper seed layer is formed is dipped into a copper plating solution including an organic accelerator and an organic suppressor are added; and

applying a positive (+) power supply having current in the range of 1 ~ 30A to the wafer.

7. The method as claimed in claim 1, wherein the copper electro-polishing process comprises:

setting a target range similar to a target plating range for forming the copper layer, in a state that a wafer in which the copper seed layer is formed is dipped into a copper plating solution including an organic accelerator, an organic suppressor and the organic leveler are added; and

applying a positive (+) power supply having current in the range of 1 ~ 30A to the wafer.

8. A method of forming a copper wiring in a semiconductor devices, the method comprising:

forming damascene patterns in an interlayer insulating film which is formed on a substrate;

sequentially forming a copper barrier metal layer and a copper seed layer on the surface of the interlayer insulating film including the damascene patterns;

performing a copper electroplating process to be filled the damascene patterns with a copper layer;

polishing the copper layer and the copper seed layer by means of a copper electro-polishing process until the copper barrier metal layer is exposed, thereby forming copper wirings within the damascene patterns; and

polishing the copper barrier metal layer by means of a chemical mechanical polishing process until the surface of the interlayer insulating film is exposed.

9. The method as claimed in claim 8, wherein the copper barrier metal layer is formed using one of ionized PVD TiN, CVD TiN, MOCVD TiN, ionized PVD Ta, ionized PVD TaN, CVD Ta, CVD TaN and CVD WN.

10. The method as claimed in claim 8, wherein the copper seed layer is formed using an ionized PVD method.

11. The method as claimed in claim 8, wherein the copper electroplating process comprises:

loading a wafer in which the copper seed layer is formed onto an electroplating apparatus in which a copper plating solution including an organic accelerator and an organic suppressor are added;

setting a plating target range so that the damascene patterns could be sufficiently filled; and

applying a negative (-) power supply having current in the range of 1 ~ 5A to the wafer.

12. The method as claimed in claim 8, wherein the copper electroplating process comprises:

loading a wafer in which the copper seed layer is formed onto an electroplating apparatus in which a copper plating solution including an organic accelerator, an organic suppressor and an organic leveler are added;

setting a plating target range so that the damascene patterns could be sufficiently filled; and

applying a negative (-) power supply having current in the range of 1 ~ 5A to the wafer.

13. The method as claimed in claim 8, wherein the copper electro-polishing process is performed by applying a positive (+) power supply having current in the range of 1 ~ 30A to the copper layer and the copper barrier metal layer, and performing the copper electro-polishing process until an electrical resistance of the copper barrier metal layer is detected and the copper electro-polishing process is self-stopped, in a state that a wafer in which the copper seed layer is formed is dipped into a copper plating solution including an organic accelerator and an organic suppressor are added.

14. The method as claimed in claim 8, wherein the copper electro-polishing process is performed by applying a positive (+) power supply having current in the range of 1 ~ 30A to the copper layer and the copper barrier metal layer, and performing the copper electro-polishing process until an electrical resistance of the copper barrier metal layer is detected and the copper electro-polishing process is self-stopped, in a state that a wafer in which the copper seed layer is formed is dipped into a copper plating solution including an organic accelerator, an organic suppressor and an organic leveler are added.